ABSTRACT OF THE DISCLOSURE

The present invention relates to a method of manufacturing a semiconductor integrated circuit in which a via hole reaching a metal wiring and a concave groove are simultaneously formed in an interlayer film. When the interlayer film and the material of an organic film embedded in the via hole are etched, the etching rate for the material of the organic film with an etching gas is set to be higher than the etching rate for the interlayer film with an etching gas. Thus, plasma etching does not proceed in a state in which the material of the organic film projects from the bottom of the concave groove formed in the interlayer film, and the production of depositions is prevented.